Rajit Manohar

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rajit@csl.cornell.edu

Education:

Ph.D. 1998	Computer Science, California Institute of Technology *Advisor: Alain J. Martin*
M.S. 1995	Computer Science, California Institute of Technology
B.S. 1994	Engineering and Applied Science, California Institute of Technology *Advisor: K. Mani Chandy*
1990–92	Computer Science and Engineering, Indian Institute of Technology, Bombay

Professional Experience:

1/2015–	**Stephen H. Weiss Presidential Fellow**	**Cornell University**
7/2012–	**Professor, ECE** *One of two founding faculty members at Cornell Tech*	**Cornell Tech**
7/2010–	**Professor, ECE**	**Cornell University**
4/2004	**Associate Professor, ECE**	
8/1998	**Assistant Professor, ECE** *Co-founder, Computer Systems Lab*	
1995–1998	**Research Assistant**	**California Institute of Technology**

Administrative

1/2015– 4/2015	**Associate Dean for Research** Cornell University's New York City Tech campus	**Cornell Tech**
11/2012– 12/2014	**Associate Dean for Academic Affairs** Founding Associate Dean at Cornell University's New York City Tech campus	**Cornell Tech**
1/2010– 6/2012	**Associate Dean for Research & Graduate Studies** College of Engineering	**Cornell University**

Sabbaticals and Leaves

8/2005– 12/2005	**Visiting Scientist** *Microsystems Technology Laboratories*	**Massachusetts Institute of Technology**
2004–2010	**Founder and CTO** *On leave from Cornell, 8/2005–7/2007*	**Achronix Semiconductor**

Honors and Awards:

Research and Technology:

2016 Inaugural Misha Mahowald Prize for Neuromorphic Engineering
For the TrueNorth project with IBM Research. The prize is for "outstanding research in neuromorphic engineering, worldwide" and is awarded to a project.

2016 Best paper finalist, ASYNC
For "Gradual Synchronization." Three finalists selected.

2016 IBM Research 2014 Pat Goldberg Math/CS/EE Best Paper Award (first place)
For "A Million Spiking-Neuron Integrated Circuit with a Scalable Communication Network and Interface." Selected annually from papers with IBM co-authors

2016 Paper selected as one of the "Best of Computer Architecture Letters" in 2015
For "Comparing Stochastic and Deterministic Computing." Four papers selected

2015 Invited "keynote" paper, IEEE Transactions on CAD
Paper: "TrueNorth: Design and Tool Flow of a 65mW 1 Million Neuron Programmable Neurosynaptic Chip"

2015 Best paper finalist, ASYNC
For "Analyzing Isochronic Forks with Potential Causality."

2014 ACM Gordon Bell Prize finalist, Supercomputing
For "Real-time Scalable Cortical Computing at 46 Giga-Synaptic OPS/Watt with ≈100× Speedup in Time-to-Solution and ≈100,000× Reduction in Energy-to-Solution"

2014 Best paper finalist, ASYNC
For "Low Power Asynchronous VLSI with NEM Relays"

2013 Best paper award, ASYNC
For "Inverting Martin Synthesis for Verification." One paper selected

2012 Best paper award, ASYNC
For "A Digital Neurosynaptic Core Using Event-Driven QDI Circuits"

2010 Best paper award, ASYNC
For "An Operand-Optimized Asynchronous IEEE 754 Double-precision floating-point adder"

2010 Best paper finalist, ASYNC
For "An Asynchronous FPGA with Two-Phase Enable Scaled Routing"

2009 IET Start-up Innovation Award, Achronix Semiconductor
For development of asynchronous FPGA technology

2007 Best paper award, High Performance Embedded Computing
For "Enabling Cognitive Architectures for UAV Mission Planning"

2006 Best paper award, ASYNC
For "A level-crossing Flash Asynchronous Analog-to-Digital Converter"

2006 Elected Fellow of the World Technology Network

2006 Globus Indus Technovators Award

2006 Invited participant, NAE Frontiers of Engineering Symposium

2005 Best paper finalist, ASYNC
For "BitSNAP: Dynamic Significance Compression for a Low-Energy Sensor Network Asynchronous Processor"

2005 IEEE Fred Ellersick Award for best unclassified paper at MILCOM
For "Dense Sensor Networks are also Energy-efficient: when more is less"

2005 MIT Technology Review's TR35: top 35 young innovators under 35
For contributions to low power microprocessor design

2004 Best paper award, IASTED Parallel and Distributed Computing and Systems
For "Δ-dataflow networks for event-stream processing"

2001 MIPS paper in Caltech Computer Science 25^{th} Anniversary Selected Bibliography.
Each Caltech CS faculty member selected two papers from their career

2000 NSF CAREER award

1996 National Semiconductor Corporation Graduate Fellowship

1993 Caltech Merit Award

1992 IIT Bombay Academic Award for being ranked 1^{st} in the Institute

1991 IIT Bombay Academic Award for being ranked 1st in the Institute

1990 Gold Medal, National Standard Examination in Physics, India

Teaching:

2016 Professor of the Year at Cornell Tech
Selected by the Cornell Tech student body; three per year across all degree programs.

2014 Stephen H. Weiss Presidential Fellow
For "a sustained record of effective, inspiring, and distinguished teaching of undergraduate students." Cornell's highest teaching honor and a permanent designation.

2012 Kenneth A. Goldman '71 Excellence in Teaching Award
One of multiple named teaching awards in the College of Engineering at Cornell

2009 Ruth and Joel Spira Excellence in Teaching Award
Department teaching award

2005 Ruth and Joel Spira Excellence in Teaching Award

2004 Michael Tien '72 Excellence in Teaching Award
One of multiple named teaching awards in the College of Engineering at Cornell

2001 Sonny Yau '72 Excellence in Teaching Award
One of multiple named teaching awards in the College of Engineering at Cornell

2001 Cornell University IEEE Teacher of the Year Award
Selected by undergraduate IEEE student chapter

2000 Tau Beta Pi and Cornell Society of Engineers Excellence in Teaching Award
One per year in the College of Engineering, selected by direct student vote

Professional Activities:

Academic:

Steering Committee Member
IEEE International Symposium on Asynchronous Circuits and Systems, 2007–2012

Associate Editor
IEEE Transactions on VLSI, 2007–2009

Program Co-Chair
11th IEEE International Symposium on Asynchronous Circuits and Systems, March 2005

Program Topic Co-Chair
Conference on Design, Automation and Test in Europe, March 2003

Program Committees
Asia and South Pacific Design Automation Conference (2016, 2017); IEEE International Conference on Event-based Control, Communication, and Signal Processing (2015, 2016); IEEE International Symposium on Asynchronous Circuits and Systems, (2001–present); International Conference on Nano-Networks (2008, 2009); International Conference on Computer Design (2006); International Conference on Computer Aided Design (2005); Conference on Design, Automation and Test in Europe (2005); International Conference on Supercomputing (2002)

Co-Organizer
Kavli Institute Symposium on Computing Challenges, Cornell, October 2008
Address-Event Workgroup, NSF Workshop on Neuromorphic Engineering, Telluride, CO, July 2000

Reviewer: Proposals and Funded Projects
Air Force Research Labs; Agency for Science, Technology, and Research, Singapore; Army Research Office; US-Israel Bi-national Science Foundation; Defense Threat Reduction Agency; IWT Brussels, Belgium; US National Science Foundation; Natural Sciences and Engineering Research Council, Canada; Singapore National Research Foundation; Swiss National Science Foundation

External Search Committees
Member of search committee for hiring chaired professors at multiple European universities.

External Review Committee
Department of Electrical and Computer Engineering, Boston University

Journal Reviewer
ACM Transactions on Programming Languages and Systems (TOPLAS); ACM Transactions on Reconfigurable Technology and Systems (TRETS); ACM Computing Surveys; Communications of the ACM (CACM); Formal Aspects of Computing (FAC); IEEE Computer; IEEE Journal of Solid-State Circuits (JSSC); IEEE Signal Processing Letters; IEEE Transactions on Circuits and Systems (TCAS); IEEE Transactions on Computer Aided Design (TCAD); IEEE Transactions on Computers (TC); IEEE Transactions on Parallel and Distributed Systems (TPDS); IEEE Transactions on VLSI (TVLSI); IET Computers and Digital Techniques; Information Processing Letters (IPL); INTEGRATION: The VLSI Journal; Nature Communications; Neural Computation (NECO); Proceedings of the IEEE

Conference Reviewer
Conference on Advanced Research in VLSI (ARVLSI); Design Automation Conference (DAC); European Conference on Parallel and Distributed Computing; International Conference on Parallel Architectures and Compilation Techniques (PACT); International Parallel Processing Symposium (IPPS); International Parallel and Distributed Processing Symposium (IPDPS); International Symposium on Asynchronous Circuits and Systems (ASYNC); International Symposium on Computer Architecture (ISCA); International Symposium on High Performance Computer Architecture (HPCA); International Symposium on Microarchitecture (MICRO); International Symposium on Operating System Principles (SOSP); ACM Symposium on Principles of Distributed Computing (PODC)

Technology Transfer:

Founder and CTO, Achronix Semiconductor
Startup company commercializing high-speed asynchronous FPGAs.
CTO 10/2004–12/2008; Chief Scientist 12/2008–4/2010; Board of Directors 10/2004–3/2011.

Asynchronous Design Tools and Methodology
Used by groups at: Achronix Semiconductor 2006–2012; IBM Research 2010–; Stanford 2014–; Qualcomm 2015–; Google 2016–

Other Activities
ATC-NY. Asynchronous logic synthesis (DARPA/SBIR). 1/2003–9/2003

Insect-Cyborg Sentinels: Technology Transfer Activity (DARPA). 6/2009–3/2011

Invited Talks and Panels:

IP and Tech Transfer

IP Strategies for Technology Entrepreneurs.
Panel, Future of Urban Innovation Summit, Columbia University, New York, NY, June 2015.

Cornell Tech Overview.
Cornell Systems-Industry Workshop, Ithaca, NY, November 2014.

Cornell NYC Tech.
ECE Department Heads Association Board of Directors Meeting, New York, NY, July 2013.

Cornell NYC Tech: New Directions in Building Human Capital.
The New York Academy of Sciences, New York, NY, April 2013.

The Cornell NYC Tech Campus.
IBM T.J. Watson Research Center, NY, March 2013.

Generation Tech: Tapping NYC's Science and Engineering Talent.
Panel discussion, The New York Academy of Sciences, New York, NY, November 2012.

Research

Stochastic vs Deterministic Computing.
Panelist, International Conference on Computer-Aided Design, Austin, TX, November 2016.

Neuromorphic Electronics.
Physics Seminar Series, IBM T.J. Watson Research Center, Yorktown Heights, NY, September 2016.

Digital Neuromorphic Systems.
*Keynote, A*STAR Neuromorphic Computing Workshop, Singapore, August 2016.*

Design Automation Challenges in Neuromorphic Systems.
Keynote, 25th International Workshop on Logic and Synthesis, Austin, TX, June 2016.

Neuromorphic Systems.
Seminar, Reservoir Labs, New York, NY, May 2016.

Comparing Stochastic and Deterministic Computing.
Best of Computer Architecture Letters Session,
IEEE Symposium on High-Performance Computer Architecture, Barcelona, Spain, March 2016.

Asynchronous Logic: A Computer Systems Perspective.
Neuro-Inspired Computational Elements (NICE) Workshop, Berkeley, CA, March 2016.

Large-Scale Neuromorphic Systems.
Triangle Computer Science Distinguished Lecturer Series, UNC/NCSU/Duke, November 2015.

Designing Massively Parallel Computing Architectures.
Neuromorphic Computing Forum, SAIT, Samsung, Korea, November 2015.

Engineering Neuromorphic Systems.
Center for Neuroengineering and Computation, Columbia University, New York, NY, September 2015.

Self-timed Neuromorphic Systems.
Computer Engineering Seminar Series, Yale University, New Haven, CT, September 2015.

Neuromorphic Systems: Past, Present, and Trends.
Computer Science Seminar, Columbia University, New York, NY, July 2015.

Digital Neuromorphic Systems.
Seminar, University of California at Berkeley, Berkeley, CA, May 2015.

Digital Neuromorphic Systems.
Workshop on Neuromorphic and Brain-based Computing Systems, Design, Automation & Test in Europe, Grenoble, France, March 2015.

Digital Neuromorphic Systems.
Physiology, Biophysics and Systems Biology Seminar, Weill Medical College, New York, NY, January 2015.

Energy Proportional Computing.
Cornell Systems-Industry Workshop, Ithaca, NY, November 2014.

Self-timed Neuromorphic Systems.
Brain-Inspired Computing, Cognitive Systems Colloquium, IBM Almaden Research Center, November 2014.

Digital Neuromorphic Electronics.
Seminar, Brain and Mind Institute, Weill Medical College, New York, NY, June 2014.

Energy-efficient self-timed circuits.
Seminar, Advanced Micro Devices, Boxborough, MA, October 2013.

Self-timed Logic for Neuromorphic Systems.
Joint EU-US Workshop on Cortical Processors, Heidelberg, Germany, October 2013.

Low power embedded systems using self-timed circuits.
Seminar, Intel STC on Embedded Computing, April 2013.

Self-timed systems: Case Studies.
2012 Kyoto Prize Symposium on Asynchronous computing, San Diego CA, March 2013.

Energy-efficient Self-timed Systems.

Qualcomm Research Center, NJ, March 2013.

Asynchronous VLSI Design.
Olin College, MA, November 2012.

Energy-Efficient Self-Timed Systems.
Case Western Reserve University, Cleveland, OH, October 2012.

Scalable Routing in Large-Scale Neuromorphic Systems.
IEEE International Conference on Engineering in Medicine and Biology
Mini-symposium on Large-scale Neuromophic Systems, August 2012.

High Performance Reconfigurable Logic.
Indian Institute of Technology, Mumbai, India, January 2012.

Digital Neuromorphic Systems.
IBM T.J. Watson Research Center, Yorktown Heights, NY, November 2011.

Asynchronous Computer Arithmetic.
Architecture seminar series, University of Wisconsin, Madison, WI, November 2011.

Ultra Low Power Computation for Secure Embedded Systems.
TRUST Autumn Conference, Washington, DC, November 2011.

Efficient floating-point: software and hardware.
Scientific Computing and Numerics Seminar, Cornell University, October 2011.

Low Power Asynchronous VLSI.
Huawei Research, Ontario, Canada, May 2011.

Activity-Driven Architecture for Neuromorphic Systems.
DARPA Neural Engineering, Science, and Technology Forum, San Diego, CA, November 2010.

Asynchronous VLSI Design.
Olin College, MA, November 2010.

Asynchronous FPGAs: An Overview.
KLA-Tencor, Milpitas, CA, October 2010.

The Technology and Business of Asynchronous FPGAs.
University of California at Berkeley, Berkeley CA, October 2010.

Self-Timed FPGAs.
Portland State University, Portland, OR, September 2010.

Reconfigurable Systems.
CS Colloquium, Cornell University, September 2010.

GHz-speed FPGAs.
CMOS Emerging Technologies Workshop, Whistler, BC, May 2010.

High-performance Reconfigurable Systems.
Visionary and Entrepreneurship Seminar, ECE, UC Davis, CA. February 2010.

The Future of FPGAs.
High Performance Embedded Computing, MIT Lincoln Labs, September 2009.

Survivor: Computer Architecture.
Panelist, High Performance Embedded Computing, MIT Lincoln Labs, September 2009.

VLSI Systems: Past, Present, and Future Trends.
California Institute of Technology, Pasadena, CA, February 2009.

Managing Design Complexity in VLSI Systems.
University of Texas at Austin, TX, February 2009.

Fault Tolerance in Asynchronous Logic.
University of Texas at Austin, TX, February 2009.

Fault Tolerance in Asynchronous Logic.
Integrated Systems Lab Seminar, Columbia University, NY, December 2008.

An Ultra Low Power Processor for Sensor Networks.
Computer Engineering Seminar, University of Texas at Austin, TX, November 2008.

Event-Driven Computing.
Center for Highly Integrated Physical Systems, Ithaca, NY, October 2008.

Fault Tolerance in Reconfigurable Fabrics.
Schloss Dagstuhl-Leibniz Center for Informatics, Wadern, Germany, September 2008.

The 50 billion transisistor challenge.
IBM Global Technology Outlook Workshop, Yorktown Heights, NY, July 2008.

Ultra Low Power Asynchronous Systems.
IBM Almaden Research Labs, San Jose, CA, June 2008.

Microprocessor Forum.
Panelist, Gilder-Forbes Telecosm Conference, Lake George, NY, May 2008.

The Critical Path of Fiberspeed Connectivity: Flexible vs Fixed Silicon Solutions.
Panelist, Gilder-Forbes Telecosm Conference, Lake George, NY, October 2007.

The Implications of Fast Asynchronous Reconfigurable Logic.
DSRC Workshop on Terascale Integration, Washington, DC, October 2007.

3D Integrated Circuits: A Designer's Perspective.
Keynote panelist, 24th VLSI Multilevel Interconnection Conference. Fremont, CA, September 2007.

Fast Reconfigurable Logic.
Yale University, September 2007.

Asynchronous FPGAs.
Keynote, Workshop on Unique Chips and Systems, San Jose, CA, April 2007.

Reconfigurable Asynchronous Logic.
University of Texas at Austin, Austin, TX, March 2007.

Asynchronous Embedded Systems.
Welch-Allyn, Skeneateles, NY, March 2007.

Asynchronous Circuits and Systems.
Pomona College, CA, November 2006.

Reconfigurable Asynchronous Logic.
Custom Integrated Circuits Conference, San Jose, CA, September 2006.

Self-timed Systems.
Microsystems Technology Labs, MIT, Boston, MA, December 2005.

Reconfigurable Asynchronous Logic.
Columbia University, New York, NY, December 2005.

Asynchronous FPGAs.
Air Force Rome Labs, Rome, NY, October 2005.

Reconfigurable Asynchronous Logic.
Olin College, MA, October 2005.

Architectures for Cognitive Systems.
Workshop on Cognitive Architectures and Systems, Ithaca, NY, July 2005.

Hardware/software co-design for Sensor Networks.
Second International Workshop on Networked Sensing Systems, San Diego, CA, June 2005.

Asynchronous Logic for Extreme Environments.
University of Central Florida, Orlando, FL, May 2005.

Asynchronous FPGAs.
Xilinx Research Labs, San Jose, CA, April 2005.

Asynchronous FPGAs.
IBM T.J. Watson Research Center, Yorktown Heights, NY, March 2005.

Activity-Driven Asynchronous Circuits and Systems.
IGERT Seminar on Machines and Organisms, Ithaca, NY, February 2005.

Issues in the Design of Sensor Network Processors.
NSF Meeting on Networks of Sensor Systems, October 2004.

Sensor Networks and Asynchronous VLSI.
IEEE Computer Society Symposium on VLSI, February 2004.

How Asynchronous should we be.
Invited panelist, IEEE Computer Society Symposium on VLSI, February 2004.

Ultra Low Power Asynchronous VLSI.
DARPA Workshop on Ultra Low Power Technologies, MIT, January 2004.

Asynchronous Event-Processing.
Analog and Biological VLSI Systems Seminar, MIT, November 2003.

SNAP: A Sensor Network Asynchronous Processor.
Electrical and Systems Engineering Colloquium, University of Pennsylvania, October 2003.

Designing an Efficient Sensor Network Processor.
VLSI seminar series, ECE, Cornell University, September 2003.

Modeling Wireless Networks with Asynchronous VLSI.
Information Sciences Seminar, California Institute of Technology, Pasadena, CA, June 2002.

Why we should design asynchronous circuits.
Intel Microprocessor Research Labs, Hillsboro, OR, April 2002.

Network Simulation with Asynchronous VLSI.
Portland State University, Portland, April 2002.

Network Simulation with Asynchronous VLSI.
AT&T Labs, Menlo Park, January 2002.

Scalable Formal Design Methods for Asynchronous VLSI.
Keynote, ACM SIGPLAN Symposium on Principles of Programming Languages, January 2002.

Asynchronous VLSI for Wireless Communication Systems.
Plenary talk, IEEE CAS Workshop on Wireless Communications and Networking, August 2001.

Low Energy Adaptive Processors.
Cornell Computer Science Distinguished Lecture Series, Ithaca, NY, September 2000.

Asynchronous VLSI Design.
NSF Workshop on Neuromorphic Engineering, Telluride, CO, July 2000.

A Methodology for Designing Asynchronous Circuits.
PRL Seminar, Cornell, January 1999.

Slack Elasticity in Asynchronous Systems.
Compaq's Systems Research Center, Palo Alto, CA, April 1998.

High-performance asynchronous microprocessors.
Cornell University (and others), March 1998.

The design of asynchronous adders.
Seminar, ECE Department, Johns Hopkins University, June 1997.

Quasi-Delay-Insensitive Circuits are Turing-Complete.
International Symposium on Asynchronous Circuits and Systems, March 1996.

Asynchronous Circuit Design.
DEC Systems Research Center, Palo Alto, September 1995.

<u>Tutorials:</u>

"Neuromorphic Asynchronous Circuits." Invited tutorial, *Neuromorphic Cognition Engineering Workshop*, Telluride, CO, 2012.

"Neuromorphic Asynchronous Circuits." Invited tutorial (with Shih-Chi Liu), *Neuromorphic Cognition Engineering Workshop*, Telluride, CO, 2011.

"Analog and Asynchronous Variation-aware Circuits for the Nanoscale Era." Tutorial (with A. B. Apsel, Alain J. Martin), *IEEE International Conference on Electronics, Circuits, and Systems*, December 2007.

Teaching Experience:

2010– **Professor** **Cornell University**

Instructor: ECE 3140: Embedded Systems*
ECE 5740: Advanced Digital VLSI
CS 5422: Physical Computing*
CS 5460: Parallel and Distributed Computing*
CS 5191: Studio
Clinic: Math for Analytics (Mathematics for Machine Learning)*

2004–2010 **Associate Professor** **Cornell University**

Instructor: ECE 5740: Advanced Digital VLSI
ECE 5710: Arithmetic Circuits*
ECE 320: Systems and Networks*

1998–2004 **Assistant Professor** **Cornell University**

Instructor: ECE 574: Advanced Digital VLSI†
EE 571: Asynchronous VLSI Design*
EE 697: Topics in Computer Systems: Dynamic Binary Translation*
ECE 474: Digital VLSI Design†
EE/CS 314: Computer Organization*

Assisted: EE 439: Digital VLSI System Design
EE 308: Fundamentals of Computer Engineering
EE 475: Computer Architecture

1996–97 **Instructor** **California Institute of Technology**

Instructor: CS 139abc: Concurrency in Computation

1993–98 **Teaching Assistant** **California Institute of Technology**

Computers, Computation, and Programs (CS20, Jan L.A. van de Snepscheut); Design and Implementation of Programming Languages (CS237, Mary W. Hall); Asynchronous VLSI Design Laboratory (CS185, Alain J. Martin); Digital VLSI Design Laboratory (CS/EE181, Alain J. Martin).

Other Teaching Experience:

2015 **Curriculum Design** **Cornell Tech**

Worked with the City University of New York's Macaulay Honors College to outline an introductory Computer Science module for their students.

2002–2005 **Explorations in Engineering** **Cornell University**

Faculty participant in Cornell's summer program for high school juniors/seniors.

2000–2001 **CURIE Academy** **Cornell University**

Faculty participant in Cornell's summer program for high school women that excel in math and science.

1996–98 **Mentor Scientist** **Caltech Pre-College Science Initiative**

* New class developed; † Significantly revised existing curriculum ($> 2/3^{\text{rd}}$).

Student volunteer for Caltech's high school teacher training program.

1994–95 **CRPC Summer Intern Advisor** **California Institute of Technology**
Suggested projects/advised summer interns in the NSF Center for Research on Parallel Computation summer internship program for women and minorities.

Advising:

Graduate Field Memberships:

Electrical and Computer Engineering; Computer Science; Applied Mathematics

Postdoctoral Advisees:

Saber Moradi, Ph.D. ETH Zurich (2015–)
Carlos Tadeo Ortega Otero, Ph.D. Cornell (2014–2015)

Ph.D. theses supervised:

Benjamin Hill (Ph.D., December 2015). *Architecture and Synthesis for Dynamically Reconfigurable Asynchronous FPGAs.* First employment: Assistant Professor, Olin College

Rob Karmazin (Ph.D., November 2015). *Automating the Physical Design of Asynchronous Circuits.* First employment: Intel

Jonathan Tse (Ph.D., September 2015). *A Simple Methodology For Design Tradeoff Analysis In Asynchronous Circuits.* First employment: Intel

Stephen Longfield (Ph.D., February 2015). *Constructive Verification of Quasi Delay-Insensitive Circuits.* First employment: Google

Carlos Tadeo Ortega Otero (Ph.D., July 2014). *Asynchronous Design for Ubiquitous Computing.* First employment: St. Jude Medical

Sandra Jackson (Ph.D., July 2014). *Gradual Synchronization.*

Nabil Imam (Ph.D., April 2014). *Canonical Neural Computations in Asynchronous Neuromorphic Circuits.* First employment: IBM Research

Benjamin Zhong Xian Tang (Ph.D., January 2014, co-advised with Prof. Bhave). *Exploiting Asynchrony in GPS Receiver Systems to Enable Ultra-Low-Power Operation.* First employment: Qualcomm

Basit Riaz Sheikh (Ph.D., August 2011). *Operand-Optimized Asynchronous Floating-Point Arithmetic.* First employment: CEO, CapitalTV, Pakistan (co-founder); Advisor to the Ministry of Information Technology and Telecom, Pakistan

Filipp Akopyan (Ph.D., April 2011). *Hybrid Synchronous/Asynchronous Design.* First employment: IBM Research

Christopher LaFrieda (Ph.D., December 2009). *Relaxed Quasi Delay-Insensitive Circuits.* First employment: Achronix Semiconductor Corporation

David Fang (Ph.D., May 2008). *A Profiling Infrastructure for Performance Evaluation of Asynchronous Systems.* First employment: Achronix Semiconductor Corporation

David Biermann (Ph.D., September 2006). *A Workload Adaptive Voltage Scaling Multiple Clock Domain Architecture.* First employment: Intel

Song Peng (Ph.D., August 2006). *Implementing Self-Healing Behavior in Quasi Delay-Insensitive Circuits.* First employment: Cadence

Virantha Ekanayake (Ph.D., May 2005). *Dynamic Significance Compression in a Sensor Network Asynchronous Processor.* First employment: Assistant Professor, Johns Hopkins University

Clinton Kelly, IV (Ph.D., May 2005). *The Design and Implementation of an Asynchronous Network on a Chip.* First employment: Achronix Semiconductor Corporation (co-founder)

John Teifel** (Ph.D., May 2004). *Fast Prototyping of Asynchronous Logic.* First employment: Senior Member of the Technical Staff, Sandia National Labs

M.S. theses supervised:

Julia Karl (M.S. December 2015). *An MSB-first Asynchronous Adder.*

Yuan Tian (M.S., May 2013). *A Parallel Implementation of Hierarchical Belief Propagation.*

Stephen Longfield (M.S., March 2013). *Design and Implementation of a Low Power Asynchronous GPS Baseband Processor.*

Carlos Otero (M.S., May 2012). *Static Power Reduction Techniques for Asynchronous Circuits.*

Nabil Imam (M.S., May 2012). *A Communication Infrastructure for Multi-Chip Neuromorphic Systems.*

Chris LaFrieda (M.S., August 2005). *Custom Quality Leaf Cell Routing Using Modern Design Rules.*

Filipp Akopyan (M.S., August 2005). *Asynchronous Analog-to-Digital Conversion.*

David Fang (M.S., October 2003). *Designing Asynchronous Register Files.*

David Biermann (M.S., December 2002). *Multiprocessor-Enabled Asynchronous Cache Controller.*

Clinton Kelly IV (M.S., November 2002). *Wireless Network Simulation Done Faster than Real Time.*

Virantha Ekanayake (M.S., November 2002). *Asynchronous DRAM Design and Implementation.*

John Teifel (M.S., May 2002). *Interchip Communication in Asynchronous VLSI Systems.*

Current graduate student advisees:

Tayyar Rzayev (Ph.D., ECE). *11/2012–*. Topic: Interactive Processors (co-advisor: David Albonesi)

Praful Purohit (Ph.D. ECE). *8/2014–*. Topic: Adaptive Imagers

Nitish Srivastava (Ph.D. ECE). *1/2015–*. Topic: Interactive Processors

Wenmian Hua (Ph.D. ECE). *1/2015–*. Topic: Timing Analysis for Asynchronous Circuits (co-advisor: Zhiru Zhang)

Sean Ogden (Ph.D. CS). *6/2015–*. Topic: Dynamic Binary Translation

External Ph.D. committees/advising:

Mika Nyström. *Asynchronous Pulse Logic*. Ph.D. CS, California Institute of Technology (2001). Advisor: Alain J. Martin

Saber Moradi. *Memory-efficient Circuits and Architectures for Asynchronous Neuromorphic Systems*. Ph.D. EE, ETH Zurich (2004). Advisor: Giacomo Indiveri

Peter Diehl. *Spike-based Learning in Cortical Networks*. Ph.D. EE, ETH Zurich (2016). Advisor: Matthew Cook

Yu Chen, Ph.D. student (EE, Columbia University). Topic: Continuous Time Digital Signal Processing. Advisor: Yannis Tsividis

Alexander Neckar, Ph.D. student (EE, Stanford University). Topic: Architectures for Neuromorphic Computing. Advisor: Kwabena Boahen

University Service:

Department:

Faculty recruiting:

ECE Faculty Search Committee for NYC faculty, 2012–2014
Faculty recruiting oversight committee, Jacobs Technion-Cornell Innovation Institute, 2013–2014
CS Faculty Search Committee, 2008–2012
Search Committee for ECE Director, 2007–2008, 2013–2014
ECE Targeted Faculty Recruiting Committees, 1998–2001, 2003–2006, 2008
ECE General Faculty Recruiting Committee, 2001–2003, 2008–2010

** Cornell nominee for the ACM Doctoral Dissertation Award.

Graduate programs:
Academic Program Director, Computer Science M.Eng. program, Cornell Tech, 2013–14
Director of Graduate Studies, ECE, 2007–2009
ECE Graduate Committee, 1999–2001, 2003–2004

Other:
Ad hoc committee member and chair for faculty promotions and reappointments (multiple)
ECE Policy Committee, 2001–2004, vice chair 2004–2005
CAM Computer Committee, Chair 2001–2004
ECE Computing Committee, 1999–2001

College and University:

Major roles:
Associate Dean for Research, Cornell Tech, 2015
Associate Dean for Academic Affairs, Cornell Tech, 2012–2014
Co-Chair, Academic Planning Committee for Cornell Tech, 2012–2013
Associate Dean for Research and Graduate Studies in Engineering, 2010–2012

Technology transfer and conflict of interest:
Member, Financial Conflict of Interest Committee, 2013–
Member, Technology Transfer Advisory Committee, 2008–2013
Operations oversight subcommittee for technology transfer office, 2008–2013
Mediation subcommittee for grievances, 2008–2013

Recruiting senior staff:
Member, search committee for the Director of Cornell's Center for Technology Licensing, 2015
Member, search committee for the Director of Cornell's Sponsored Programs Office, 2010, 2013

Graduate studies:
Member, Graduate Education Planning Task Force, 2009
Member, Research Advisory Group for Engineering, 2008–2009
Member, Review committee, Graduate School TOEFL Requirements, 2008–2012
Graduate Admissions Advisory Board, 2005

Teaching:
Advisory Board Member, Center for Teaching Excellence, 2011–2013
College of Engineering Teaching Awards Committee, 2003

PUBLICATIONS

(underlined names are my students)

Book Chapter Contributions:

Communication. Chapter 2 in "Event-based Neuromorphic Systems." Wiley, 2015.

Towards Large-Scale Neuromorphic Systems. Chapter 16 in "Event-based Neuromorphic Systems." Wiley, 2015.

Articles:

Filipp Akopyan, Carlos Tadeo Ortega Otero, and Rajit Manohar. Hybrid Synchronous-Asynchronous Tool Flow for Emerging VLSI Design. *IEEE International Workshop on Logic Synthesis*, June 2016.

Sandra Jackson and Rajit Manohar. Gradual Synchronization. *IEEE International Symposium on Asynchronous Circuits and Systems*, May 2016. (**Best paper finalist**)

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