Cornell NYC Tech, future campus on Roosevelt Island, New York, NY

Selected Publications

Stephen Longfield, Brittany Nkounkou, Rajit Manohar, and Ross Tate. **Preventing Glitches and Short Circuits in High-Level Self-Timed Chip Specifications.** *36th Annual ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2015.

Rajit Manohar and Yoram Moses. **Analyzing Isochronic Forks with Potential Causality.** *IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, May 2015.

Robert Karmazin, Stephen Longfield, Carlos Tadeo Ortega Otero, and Rajit Manohar. **Timing Driven Placement for Quasi Delay-Insensitive Circuits.** *IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, May 2015.

A. Cassidy, R. Alvarez-Icaza, F. Akopyan et al. **Real-Time Scalable Cortical Computing at 46 Giga-Synaptic OPS/Watt with ~100x Speedup in Time-to-Solution and ~100,000x Reduction in Energy-to-Solution.** *Proc. Supercomputing (SC2014),* November 2014.

Stephen Longfield and Rajit Manohar. **Removing Concurrency for Rapid Functional Verification.** *Proceedings of the 2014 International Conference on Computer-Aided Design (ICCAD)*, November 2014.

P. Merolla, J. Arthur, R. Alvarez-Icaza et al. **A Million Spiking Neuron Integrated Circuit with a Scalable Communication Network and Interface.** *Science, **345**(6197):668-673,* August 2014.

Carlos Tadeo Ortega Otero, Jonathan Tse, Robert Karmazin, Benjamin Hill, Rajit Manohar. **ULSNAP: An Ultra-low Power Event-Driven Microcontroller for Sensor Network Nodes.** *Proc. IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2014.

AVLSI

Cornell University

Asynchronous VLSI and Architecture

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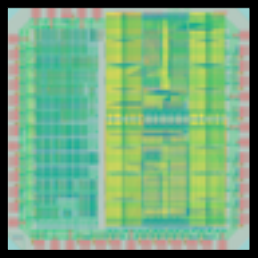

ULSNAP processor

TrueNorth neuromorphic chip

Asynchronous FPGA

Group Overview

The asynchronous VLSI and architecture group is part of Cornell's Computer Systems Lab. The group studies both fully asynchronous and partially asynchronous systems with the goal of improving overall efficiency at the circuit, architecture, and algorithmic level.

The group conducts research on all aspects of asynchronous design, including the theory of concurrent systems, circuits, architecture, and design automation. Our ideas are validated by designing chips that demonstrate significant improvements in system efficiency.

Managing design complexity is another theme that underlies our research. Design methods for asynchronous VLSI are amenable to formal analysis, enabling a chip design methodology where circuits are correct-by-construction.

Rajit Manohar leads the asynchronous VLSI and architecture group. He received his B.S., M.S., and Ph.D. from Caltech. He founded Cornell's Computer Systems Lab in 1998, and is currently Professor of Electrical and Computer Engineering, a member of the graduate fields of Computer Science and Applied Mathematics, and an affiliate of the Cognitive Studies and Neuroscience programs.

Research Areas

Neuromorphic Systems

In spite of the incredible performance of mainstream processors, humans routinely outperform computers in many tasks. The goal of this project is to develop architectures and systems that can achieve human performance for cognitive tasks. Topics include associative memory architectures, massively parallel tiled architectures, learning and inference in VLSI, and electronic models of neurons, synapses, and axons.

Ultra Low Power Embedded Systems

Untethered systems such as sensors, mobile phones, and digital music players are energy-constrained. The goal of this project is to develop circuit and architectural techniques to dramatically reduce the energy requirements for a wide variety of embedded systems. Topics include ultra low power microprocessors, signal processing, GPS, and security.

FPGAs and Reconfigurable Systems

Programmable asynchronous pipelines have the potential to dramatically improve the performance of reconfigurable systems. The goal of this project is to develop FPGA architectures that demonstrate application throughput in the multi-GHz range in standard CMOS technologies. Topics include high-throughput dynamic logic, voltage scaling, synthesis and automation, FPGA architecture, and dynamic reconfiguration.

Energy-Efficient VLSI and Architecture

In spite of progress in electronics, mobile platforms have a lifetime that is measured in days rather than months. The goal of this project is to create systems with GHz-class performance that have months of battery life in the context of information appliances like e-books. Topics include user behavior analysis, heterogeneous micro-architecture, efficient arithmetic circuits, and self-aware interfaces.